UNIVERSITEIT GENT

THALES

INRIA FUTURS

Opening Up Automatic Structural Design Space Exploration by Fixing Modular Simulation

VEERLE DESMET *Ghent University*

SYLVAIN GIRBAL *Thales TRT*

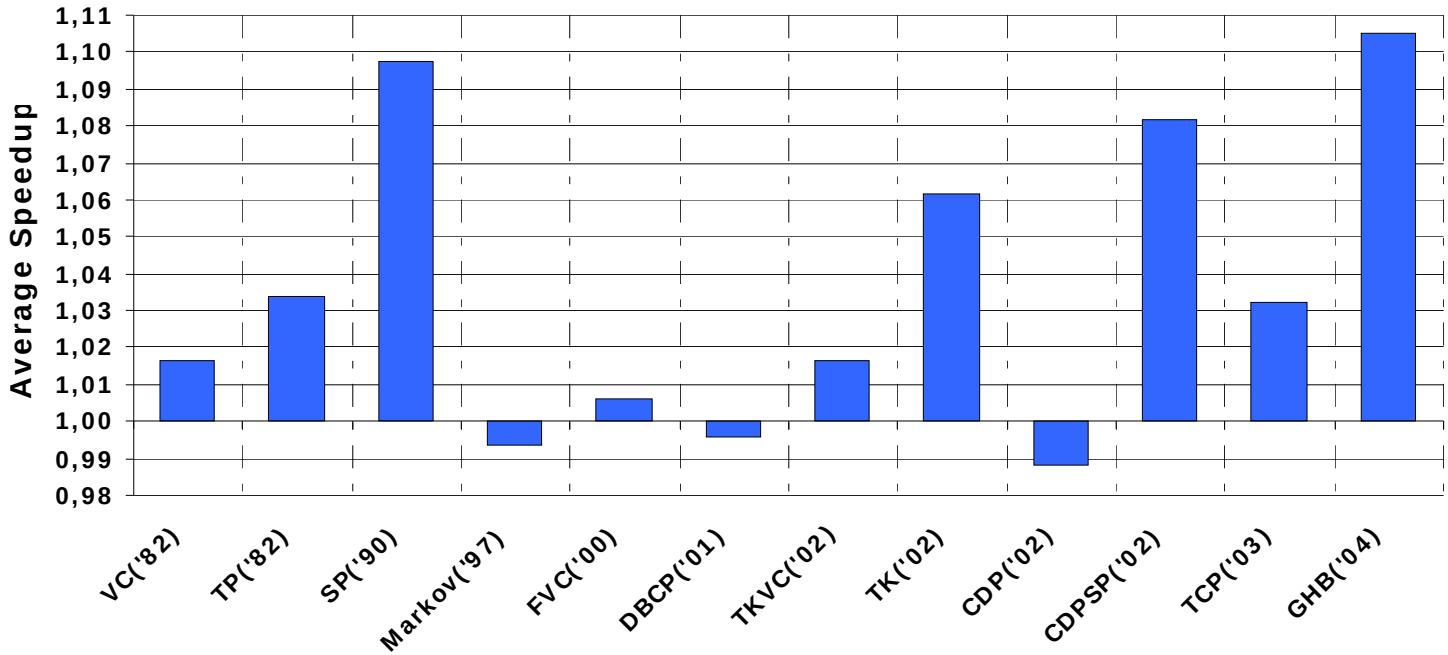
OLIVIER TE M *INRIA*

SARC
SCALABLE COMPUTER ARCHITECTURE

HiPEAC
COMPILATION ECTURE

Motivation

Need for systematic quantitative comparison



[MICRO 2004, Gracia-Pérez et al.]

Computer Architecture Research

IDEA

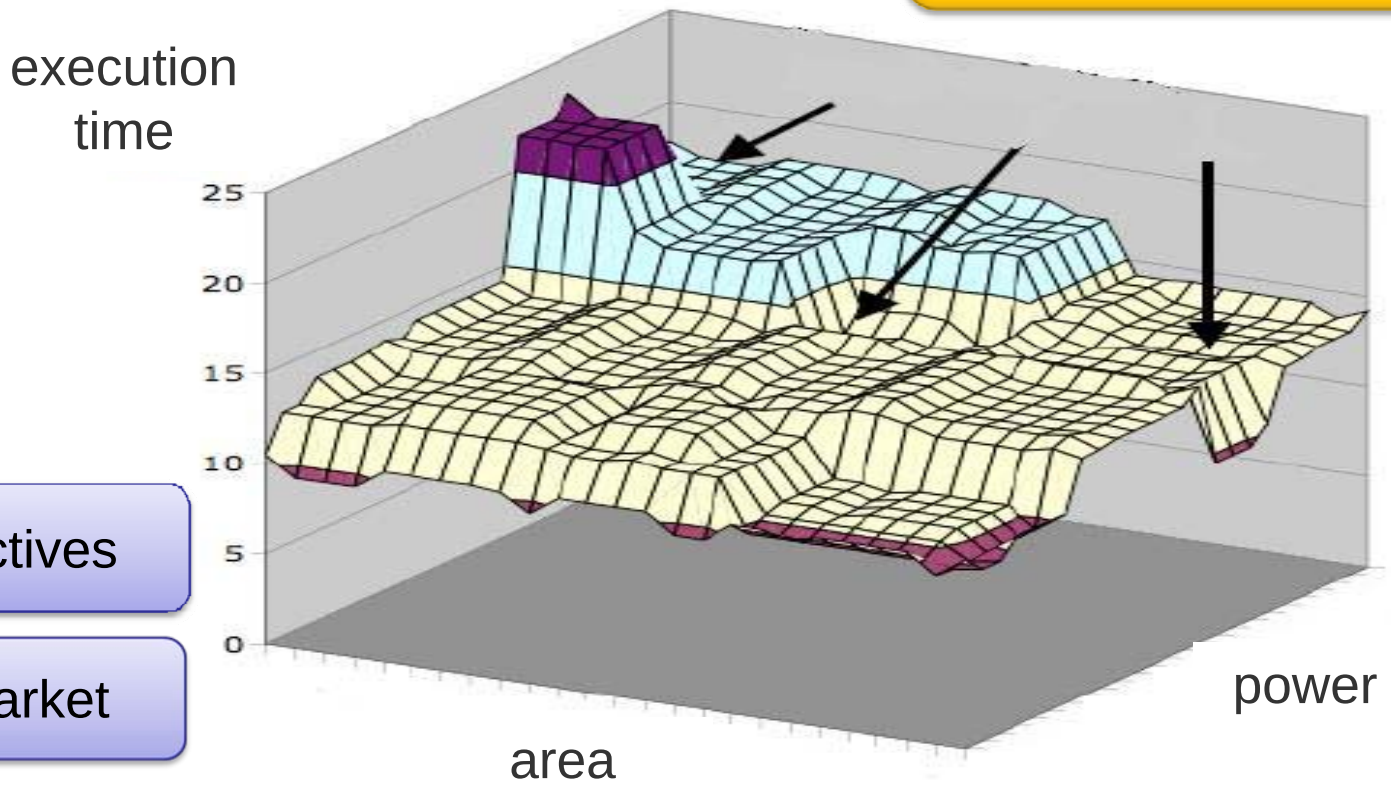
FAIR COMPARISON

REPRODUCTION EXISTING TECHNIQUES

EXPLORATION

Design space exploration: need more than intuition and experience?

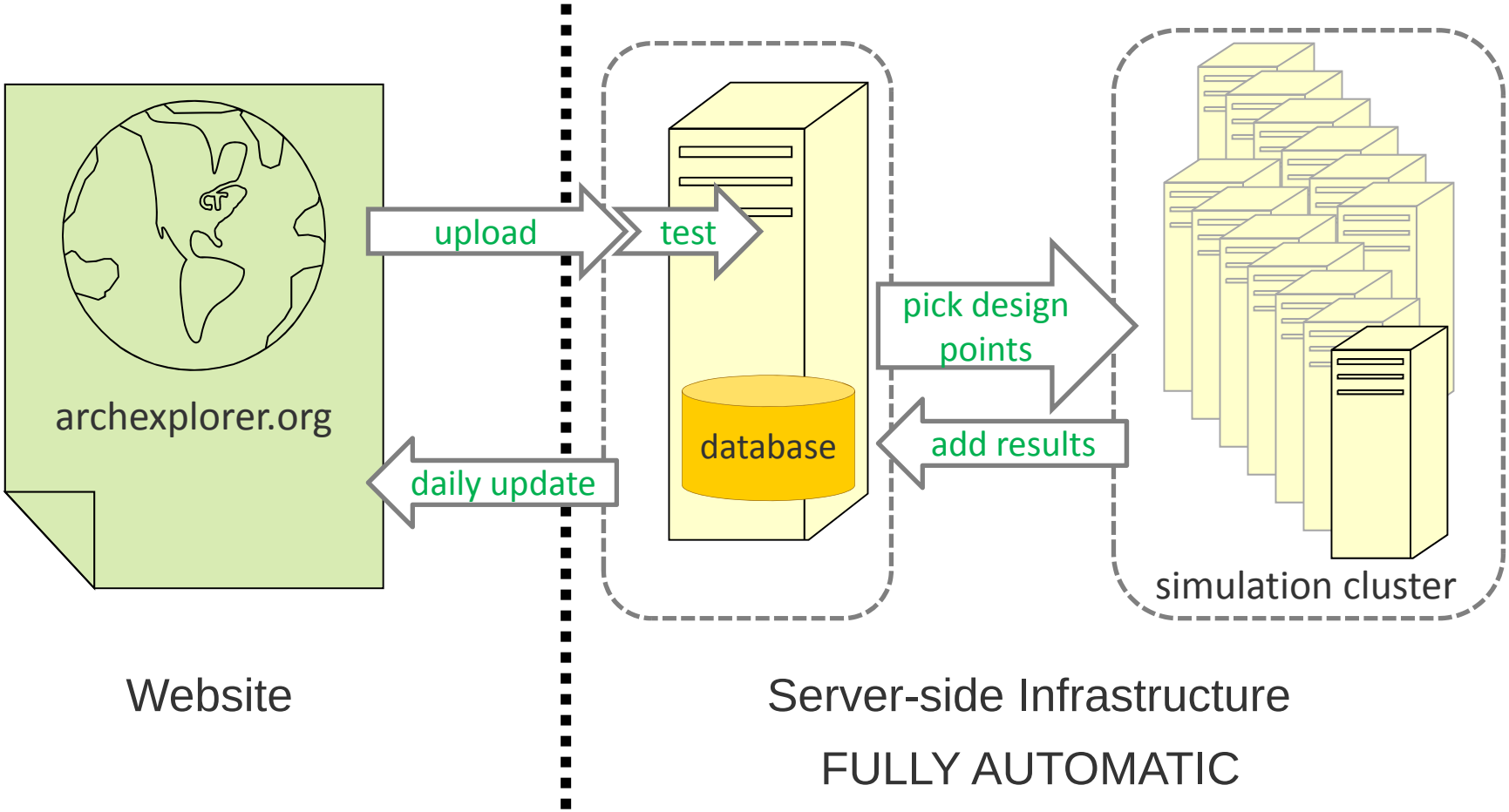
AUTOMATIC EXPLORATION



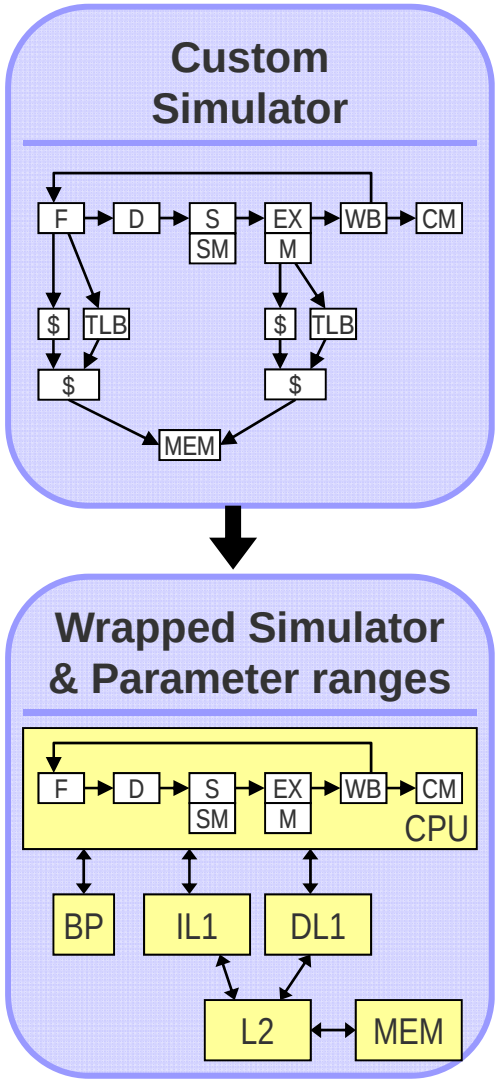
Multi-objectives

Time-to-market

ArchExplorer: repository + automatic exploration

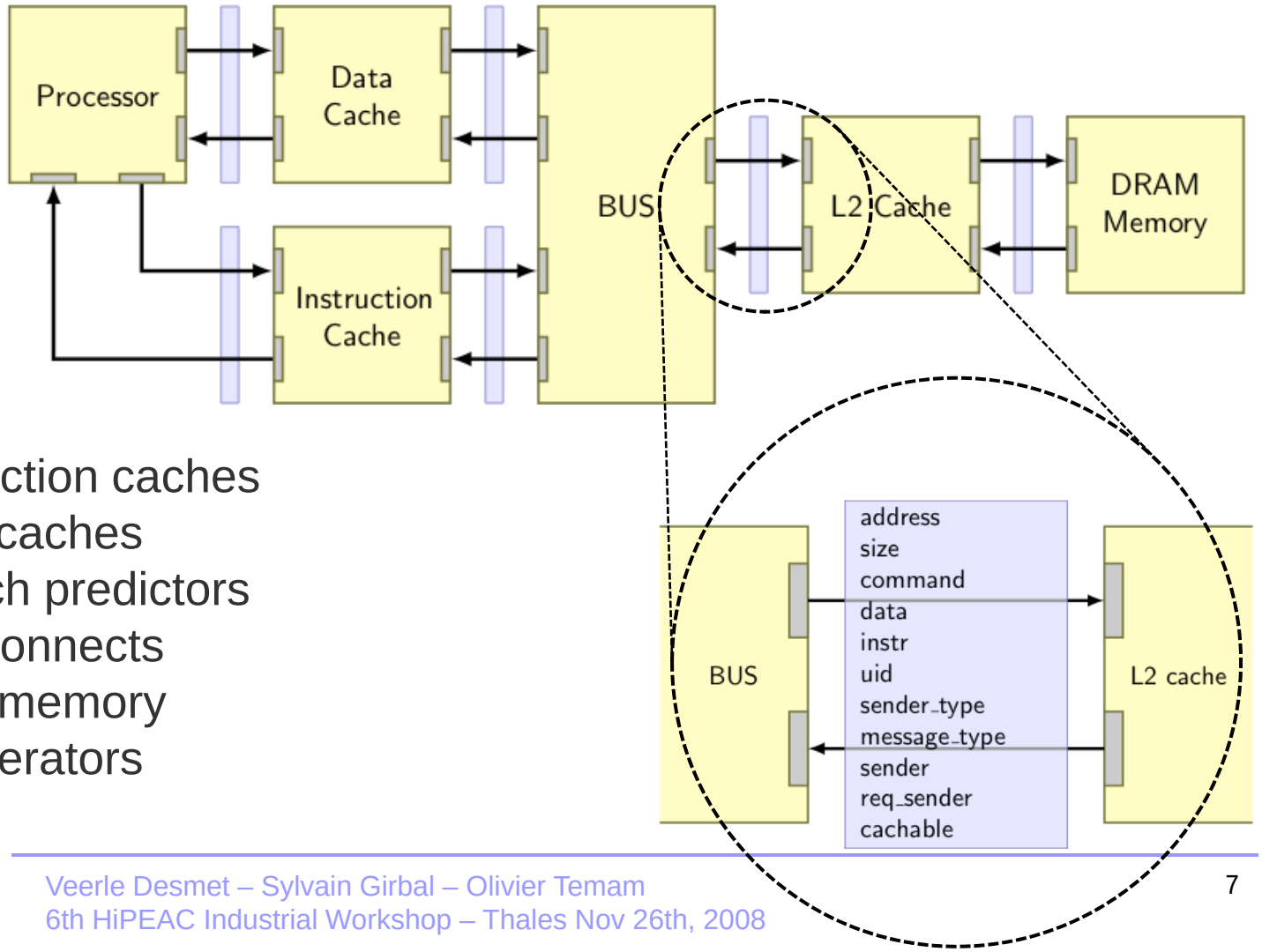


How to compare?



1. Custom simulator
2. Hardware compatibility
3. Software compatibility
4. Upload

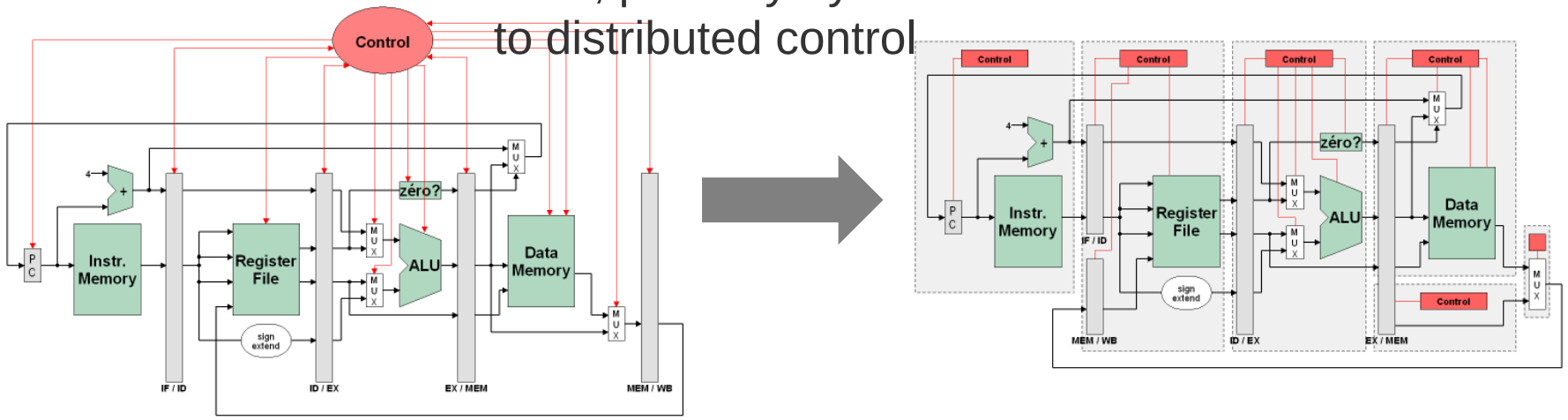
Hardware compatibility



Instruction caches
Data caches
Branch predictors
Interconnects
Main memory
Accelerators
...

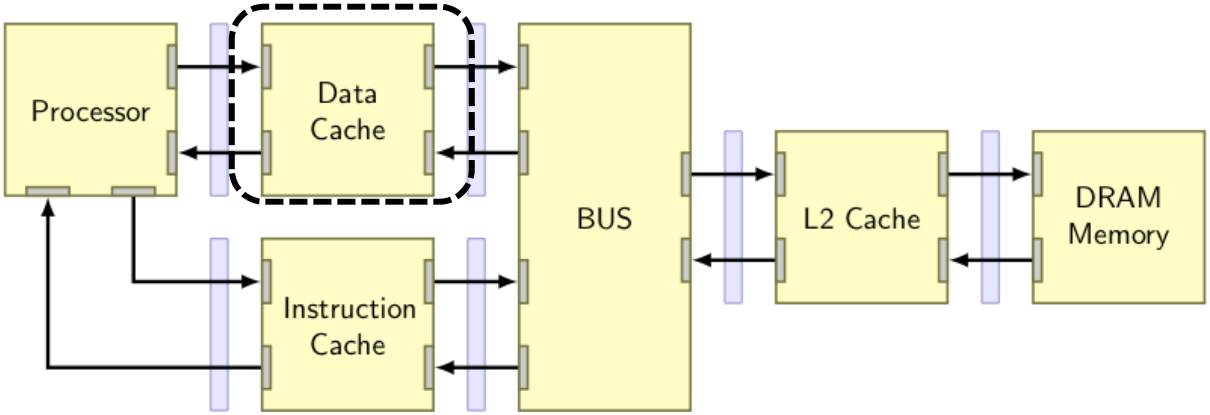
Software compatibility

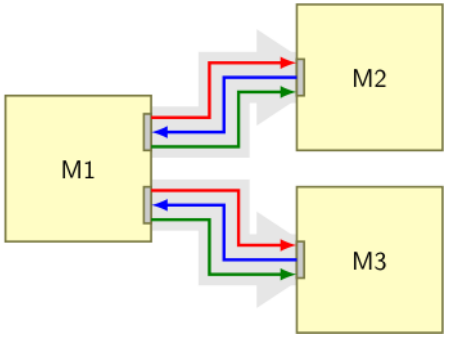
Isolate the hardware block, possibly by from centralized control to distributed control



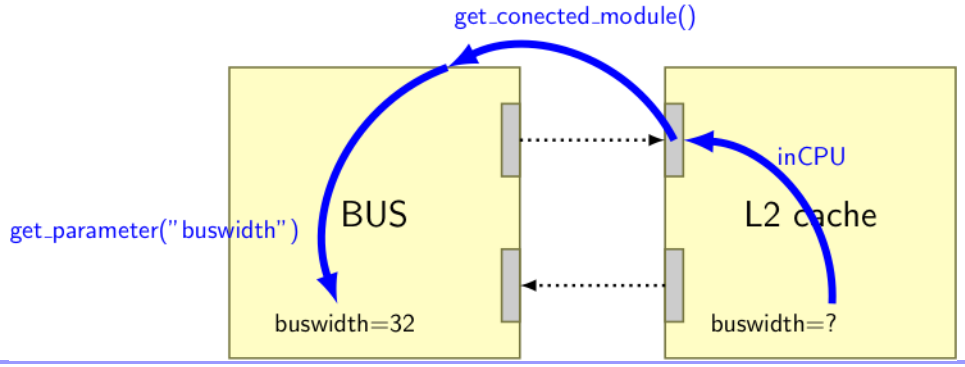
Software compatibility

Wrapping in SystemC-based on UNISIM communication layer
Models of computation

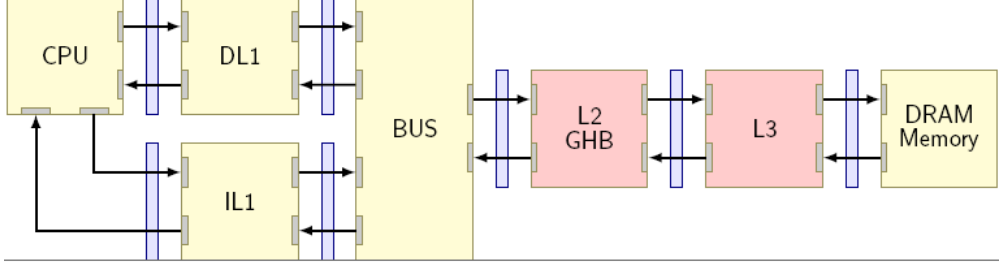




Self-Configuration and parameters legality



Case study

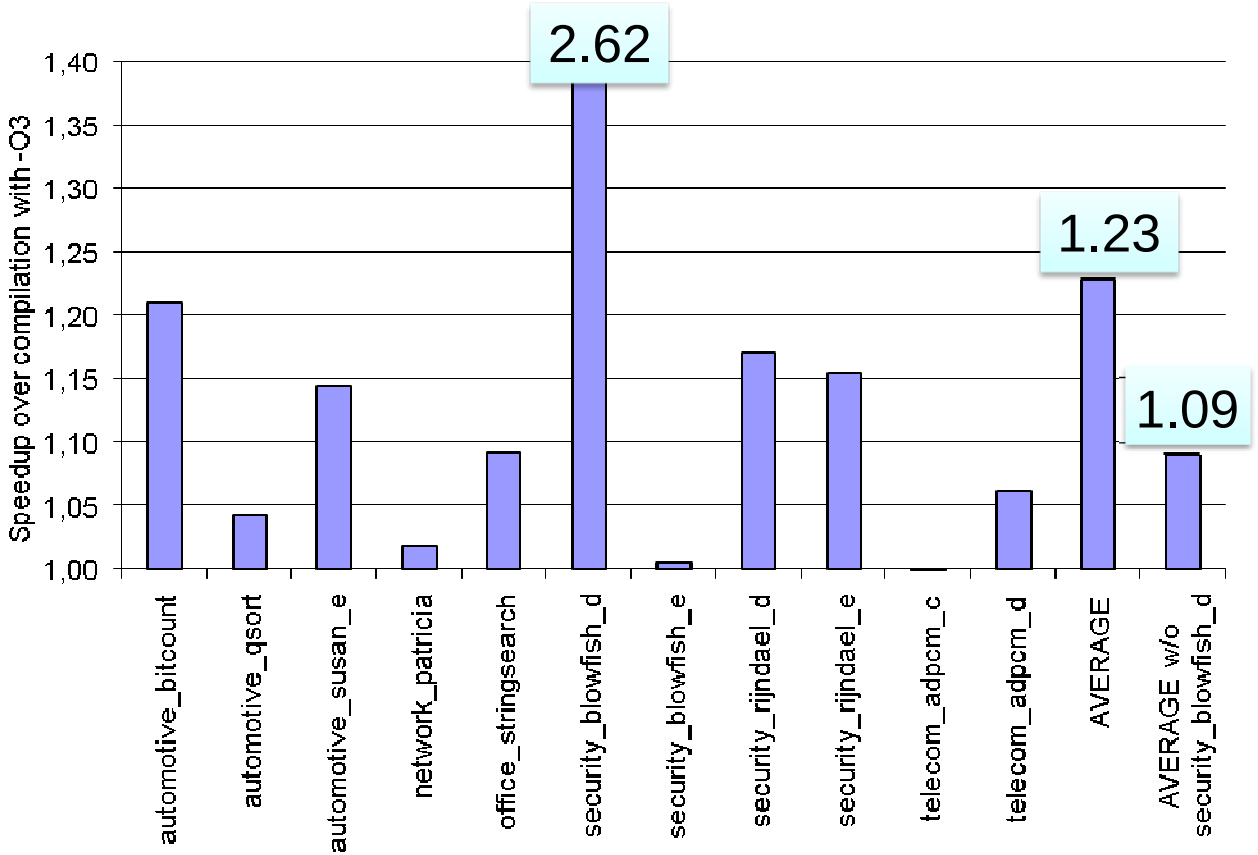


Memory sub-system for embedded processor

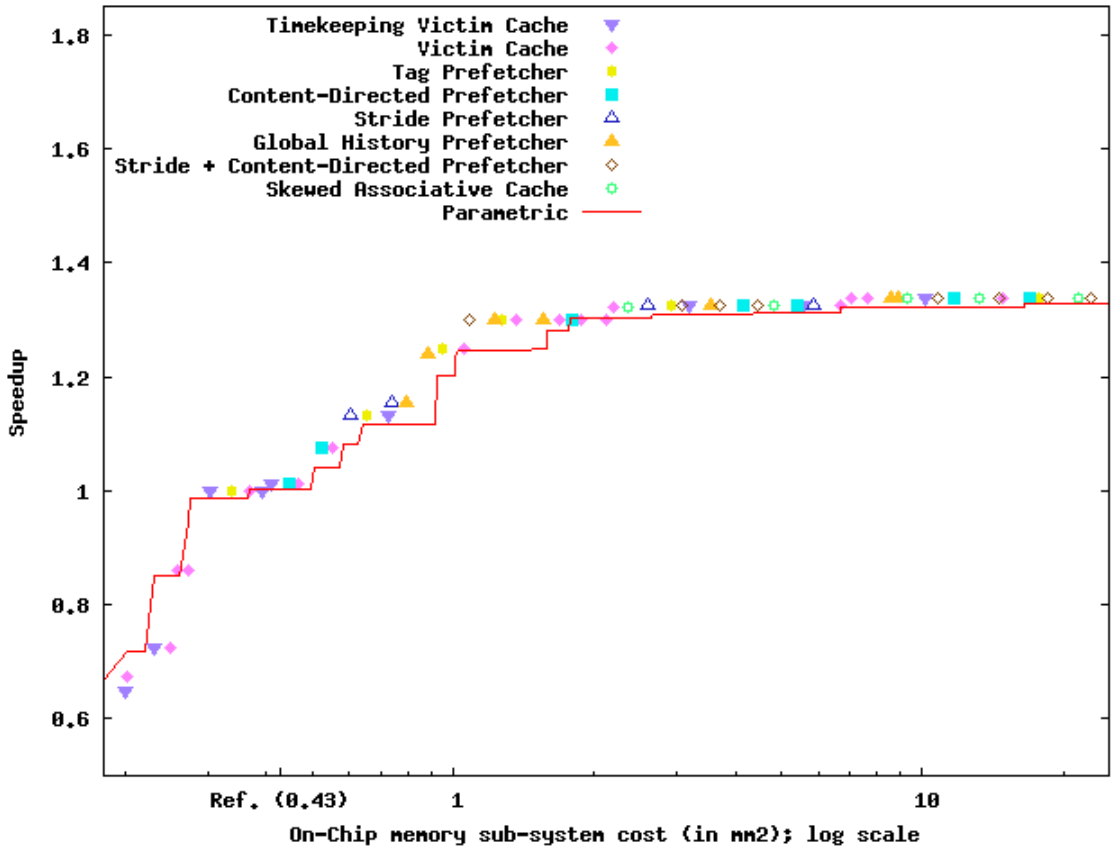
- PowerPC405
- 8 different cache modules available
- Complex hierarchies automatically explored
- Ranking designs for performance, power, energy, area,...

Victim Cache
Timekeeping Victim cache
Stride Prefetcher
Content-Directed Prefetcher
Stride + Content Directed Prefetcher
Tag Prefetcher
Global History Prefetcher
Skewed associtiative cache

Accurate comparison needs compiler tuning as well



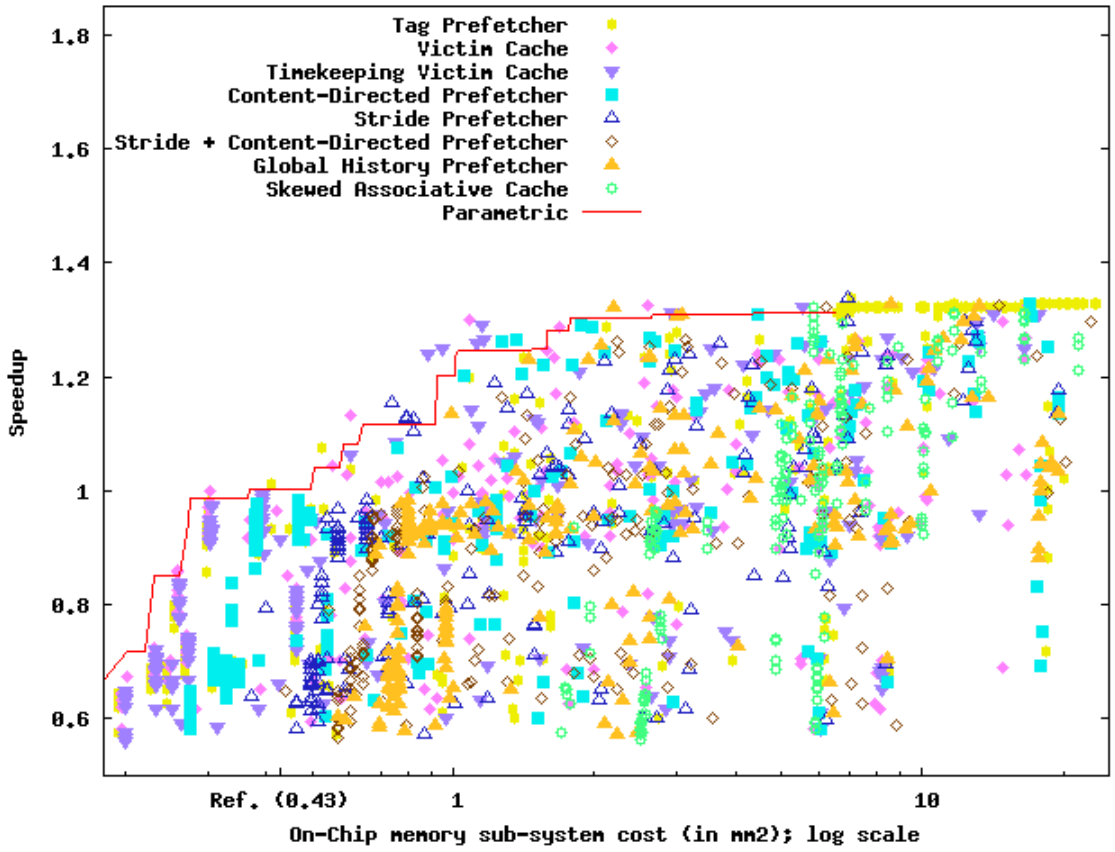
Best data cache mechanisms per area



CONCLUSIONS:

1. Contrast to Gracia-Pérez et al. [MICRO 2004]
2. No clear winner
3. Close to tuned parametric cache

Best data cache mechanisms per area



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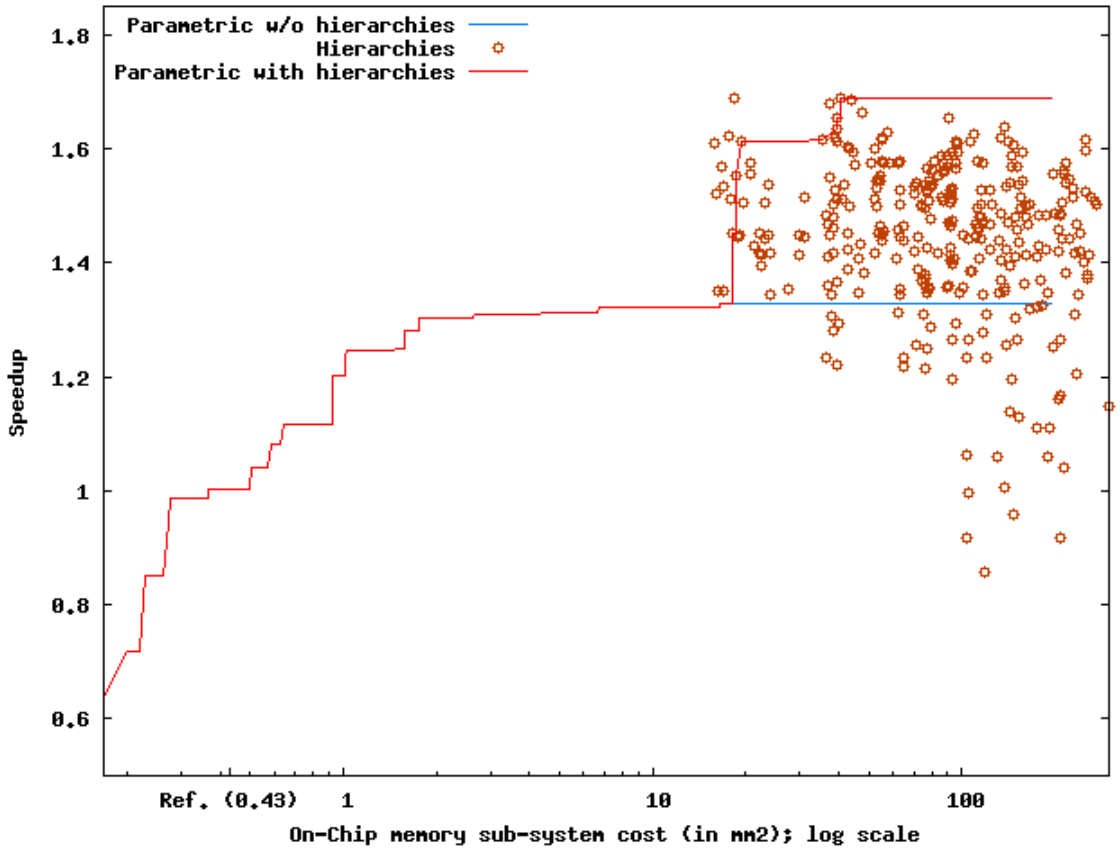
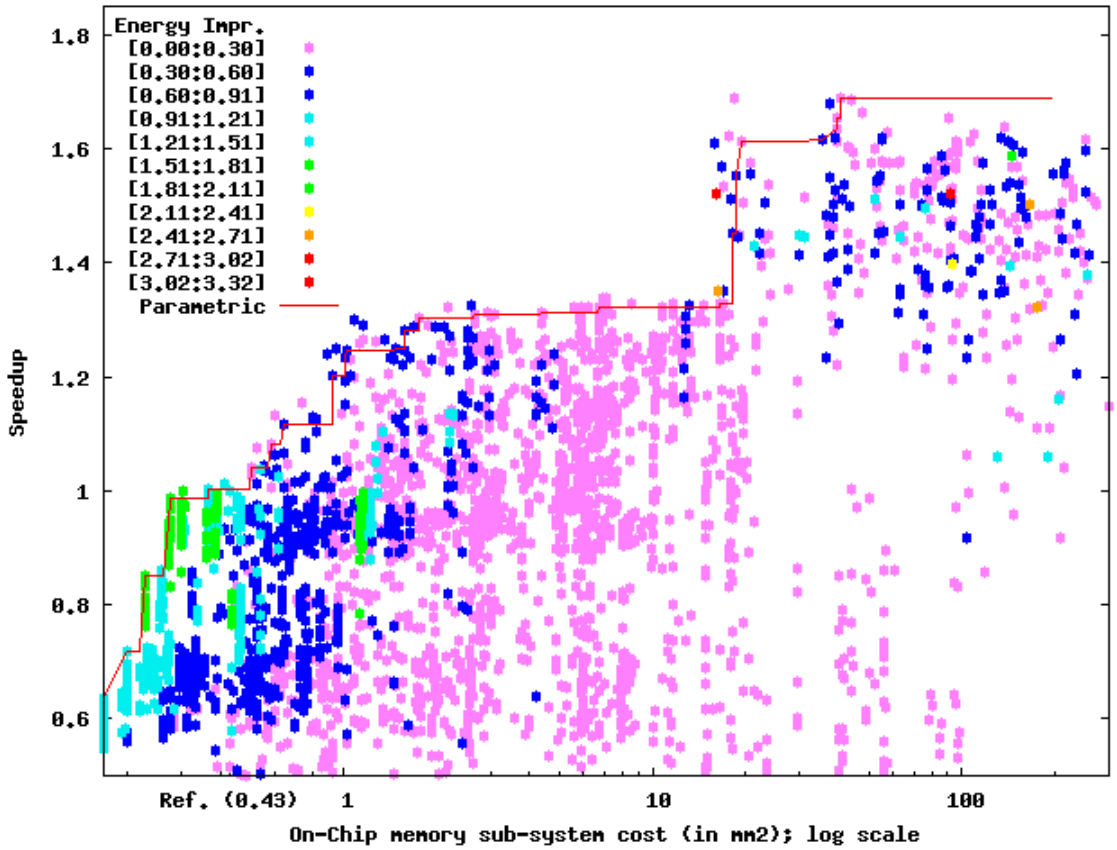
Composing cache hierarchies



Speedup and Energy Improvement



Check out this website:

ARCHEXPLORER.ORG

Permanent on-line competition - Mozilla Firefox

File Edit View History Bookmarks Tools Help

http://archexplorer.org/ranking.html

Google Agenda Cambridge

Google Agenda | Permanent on-line competition | Gmail - Inbox - veerle.desmet@g... | E-mail :: Inbox | Start Orange wifi access

Design Space Exploration

Permanent on-line competition(s)

Home | Ranking | Download | HowTo | Participate

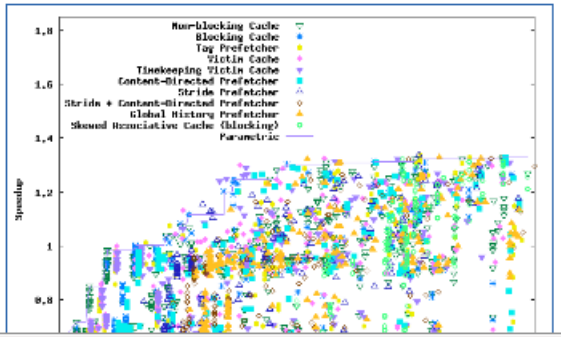
Last updated: Tue Nov 25 22:08:12 CET 2008

Participate and evaluate your own mechanisms

Ranking of available cache mechanisms

Only top points, i.e. points that are above the parametric envelope either performance-wise or energy-wise, are listed. To sort, click on column title.

Cache Mechanism	Area in mm2 (memory subsystem only)	Speedup (over PowerPC405)	Energy Improvement (over PowerPC405)
Stride Prefetcher [8]	6.938	1.339	0.046
Tag Prefetcher [7]	7.050	1.339	0.047
Tag Prefetcher [7]	11.714	1.328	0.046
Global History Prefetcher [9]	8.568	1.327	0.046
Stride + Content-Directed Prefetcher [12]	14.609	1.327	0.148
Victim Cache	2.601	1.326	0.572



http://archexplorer.org/fig_parametric_structural.pdf

Conclusion

- Permanent open competition(s)
- Future:
  - superscalar processor
  - branch predictor repository
  - multi-cores
- Open for your ideas!
  - NoC, compiler extensions,...

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